User's Guide

NHD-16032BZ-FSW-GBW

LCM

(Liquid Crystal Display Graphic Module)

RoHS Compliant

NHD-	Newhaven Display
16032-	160 x 32 pixels
BZ-	Version Line
F-	Transflective
SW-	Side White LED B/L
G-	STN- Gray
B-	6:00 View
W-	Wide Temperature (-20 ~ +70c)

For product support, contact

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2511 Technology Drive, #101
Elgin, IL 60124
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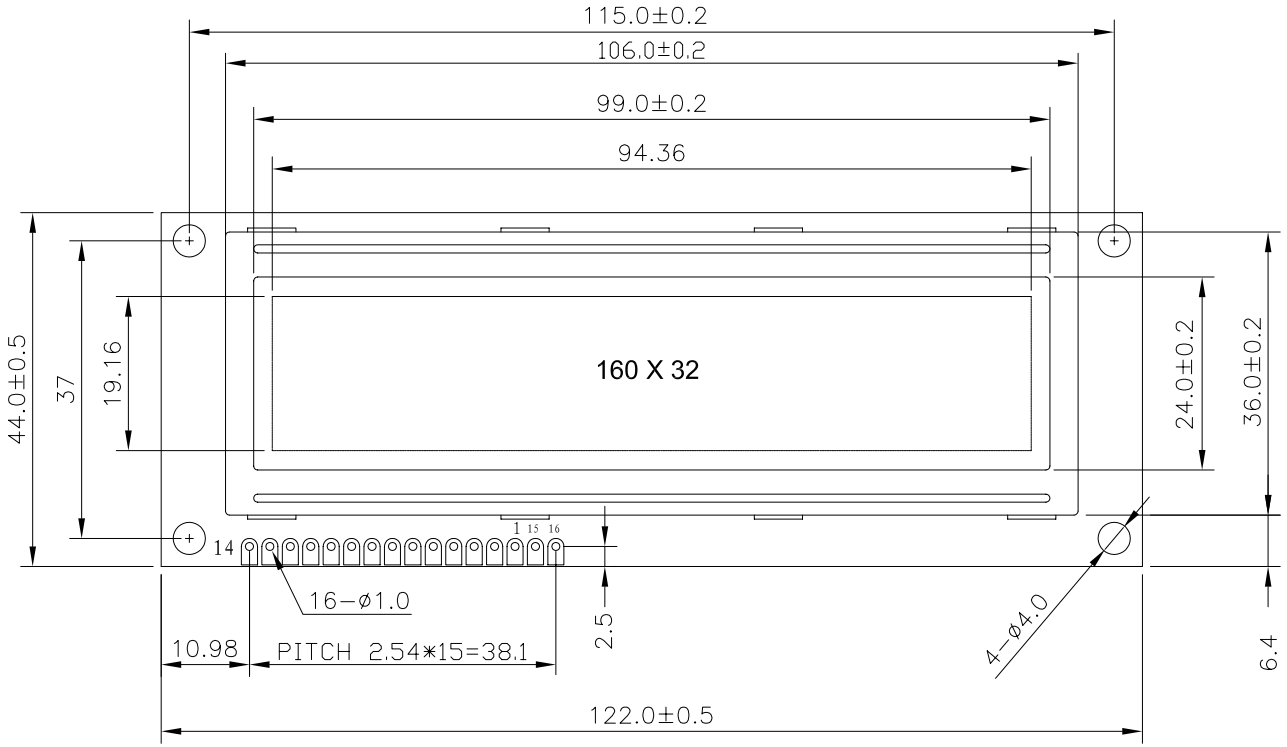
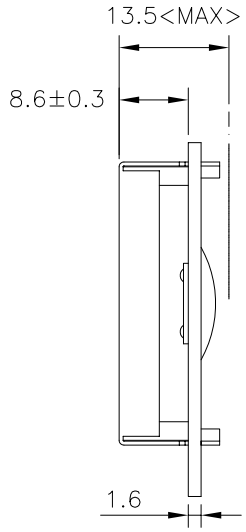
February 29, 2008

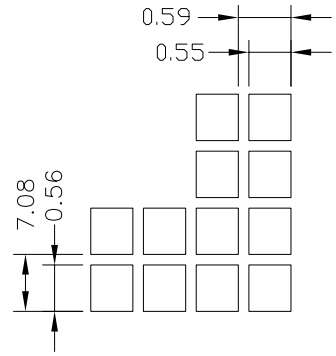
REV	DESCRIPTION:	DATE





PIN ASSIGNMENT

1	VSS
2	VDD
3	NC
4	RS
5	R/W
6	E
7~14	DB0~DB7
15	LED+
16	LED-



Specification:

1). Driving: Duty:1/32, Bias:1/6, VLCD:4.8V, VDD:3.0V
2). Viewing Direction: 6 O'clock
3). Display mode: STN Gray /Transflective
4). Operating temp.: −20°c~+70°C
Storage temp.: −30°c~+80°C
5). Driver : ST7920
6). Backlight: White/5.0V

Model Name: NHD-16032BZ-FSW-GBW		Newhaven Display	
GENERAL TOL: ± 0.2			
APPROVALS	DATE	DRAWN NO.	SCALE: 1:1
DWN: Qiqei Qiu			
CHK:		SIZE: A4	UNIT: mm / Page: 1-1
APP: Guoxiang Ye			

Item	Symbol	Min	Max	Unit
Power Voltage	V_{DD}-V_{SS}	0	7.0	V
Input Voltage	V_O	V_{SS}	V_{DD}	
Operating Temperature Range	V_{OP}	-20	+70	℃
Storage Temperature Range	T_{ST}	-30	+80	

*Wide Temperature range is available

(operating/storage temperature as wide as -20～+70/-30～+80℃)。

3. Description Of Terminals

Pin No.	Pin Name	Input/ Output	External Connection	Function
1	VSS	—	Power Supply	VSS: GND
2	VDD	—		VDD: +5V
3	VO	—		V_{LCD} adjustment
4	RS	INPUT	MPU	Register select signal "0":Instruction register (when writing) Busy flag & address counter (When reading) "1":Data register (when writing & reading)
5	R/W	Input	MPU	Read/write select signal "0" for writing , "1" for reading
6	E	Input	MPU	Operation (data read/write) enable signal
7 / 10	DB0-DB3	Input	MPU	Low-order lines of data bus with 3-state, bi-directional function for use in data transaction with the MPU. These lines are not used when interfacing with a 4-bit microprocessor.
11 / 14	DB4-DB7	Input	MPU	High-order lines of data bus with 3-state, bi-directional function for use in data transactions with the MPU. DB7 may also be used to check the busy flag.
15 / 16	LED "+" LED "-"	Input	BACKLIGHT SUPPLY POWER	LED "A" VOLTAGE V=5.0V with 68ohm on-board resistor LED "K" : GND

4. Optical Characteristics

For STN Type Display Module (T_a=25℃, V_{DD}=5.0V±0.25V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	$C_r \geqslant 2$	-60	—	35	deg
	Φ		-40	—	40	
Contrast ratio	C_r		—	6	—	—
Response time(rise)	T_r	—	—	150	250	ms
Response time(fall)	T_r	—	—	150	250	ms

5. Electrical Characteristics

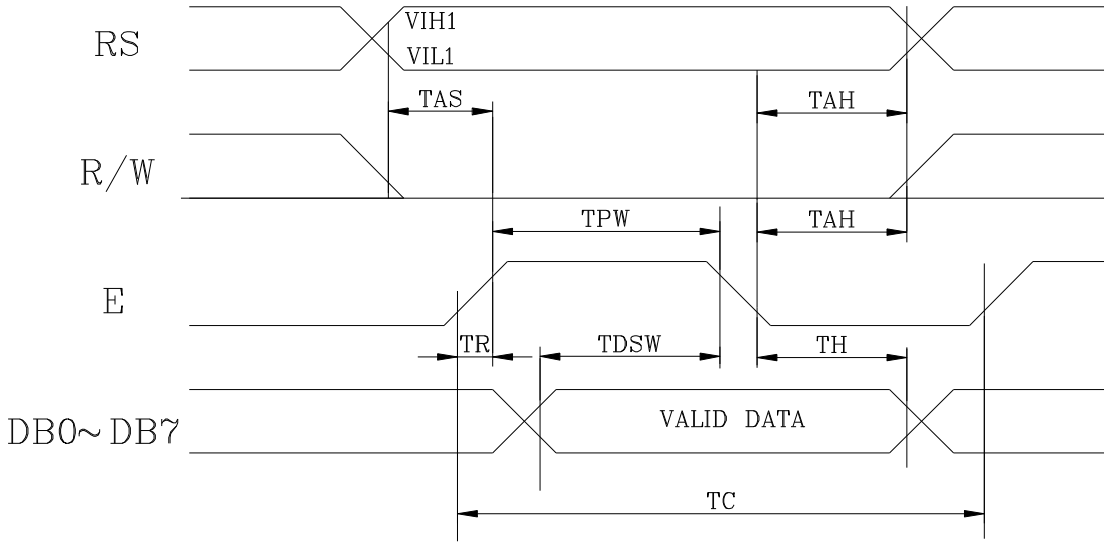
DC Characteristics

Parameter	Symbol	Conditions	Min.	Type	Max.	Unit
Supply voltage for LCD	$V_{DD}-V_O$	T_A=25℃	—	4.6	—	V
Input voltage	V_{DD}		4.7	—	5.5	V
Supply current	I_{DD}	V_{DD}=5.0V;T_A=25℃	—	1.5	2.5	mA
Input leakage current	I_{LKG}		—	—	1.0	μA
"H" level input voltage	V_{IH}		2.2	—	V_{DD}	V
"L" level input voltage	V_{IL}	Twice initial value or less	0	—	0.6	V
"H" level output voltage	V_{OH}	LOH= -0.25mA	2.4	—	—	V
"L" level output voltage	V_{OL}	LOL=1.6mA	—	—	0.4	V
Backlight supply voltage	V_F		—	4.2	4.5	V

l AC characteristics(VDD=5V,Ta=25℃)

Symbol	characteristics	Test condition	Min.	Typ.	Max.	Unit
Fosc	OSC frequency	Rf=39k	480	540	600	KHZ

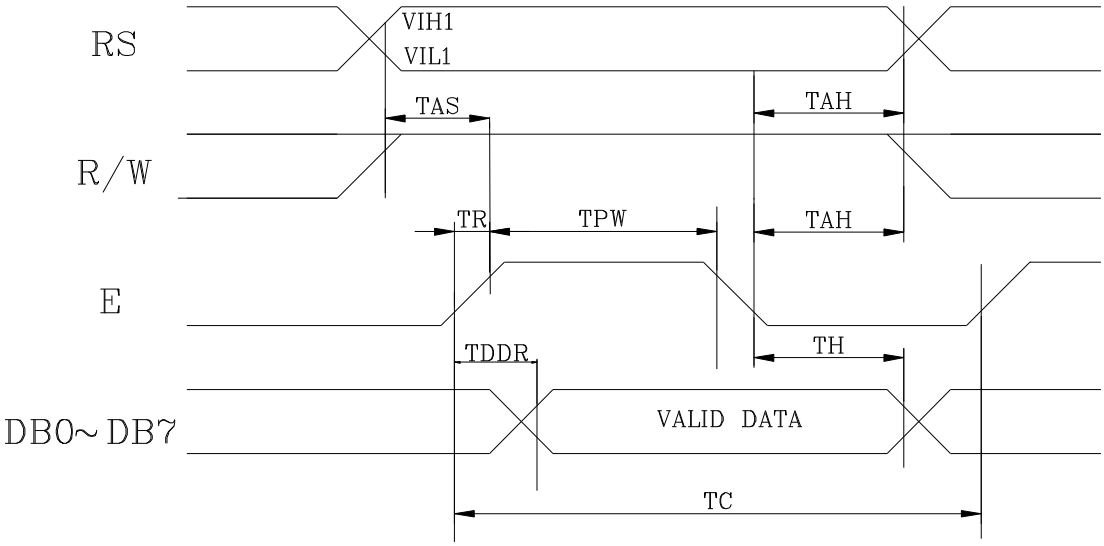
Write timing



FOR WRITE MODE (WRITING DATA FROM MPU TO ST7920)

PARAMETER	SYMBOL	MESURE TIME	UNIT
system cycle time	TC	13,000	ns
address setup time	TAS	1,500	ns
Address hold time	TAH	1,500	ns
Data setup time	TDSW	1,000	ns
Data hold time	TH	20	ns
Enable pulsewidth	TPW	1,500	ns
Enable rise/fall time	TR,TF	25	ns

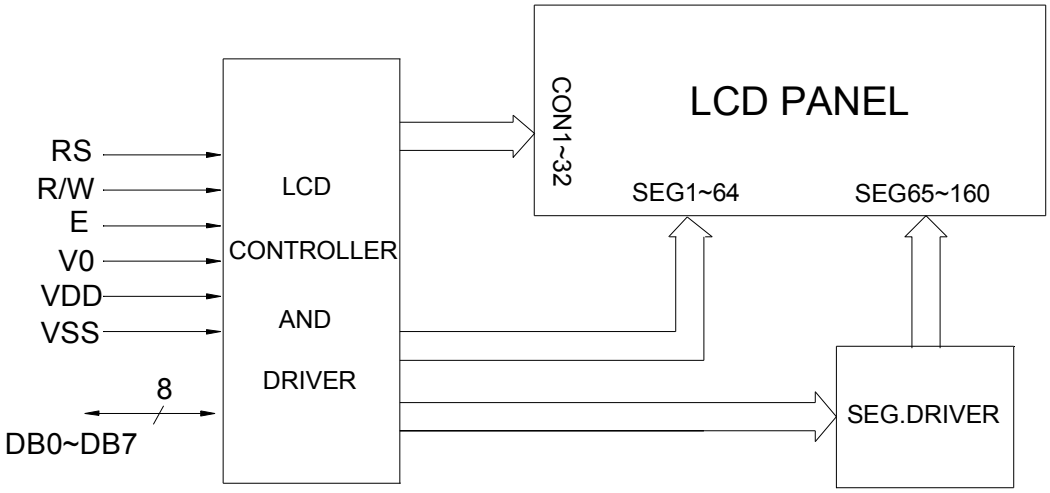
Read Timing

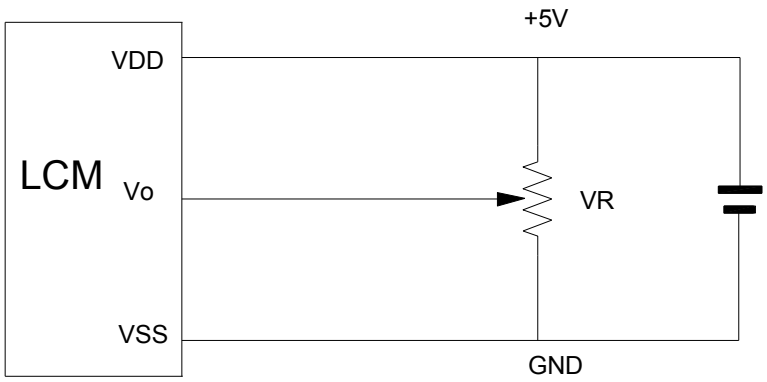


FOR READ MODE(READING DATA FORM ST7920 TO MPU)

PARAMETER	SYMBOL	MESURE TIME	UNIT
system cycle time	TC	13,000	ns
address setup time	TAS	1,500	ns
Address hold time	TAH	1,500	ns
Data setup time	TDDR	1,000	ns
Data hold time	TH	20	ns
Enable pulsewidth	TPW	1,500	ns
Enable rise/fall time	TR,TF	25	ns

6. Block digram





VDD-Vo:LCD DRIVING VOLTAGE
VR:10K~20K

Character Generator ROM (CGROM)

The character generator ROM generates 16 x 16 dot or 16 x 8 dot character patterns from two 8-bit character codes. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CGRAM)

In the character generator RAM, the user can rewrite character patterns by program. For 16 x 16 dots, four character patterns can be written.

See Table 1 for the relationship between CGRAM addresses and data and display patterns. Areas they are not used for display can be used as general data RAM.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPUaccess are generated separately to avoid interfering with each other. Therefore, when writing data toDDRAM, for example, there will be no undesirable interference, such as flickering, in areas other thanthe display area.

LCD Driver Circuit

LCD Driver circuit has 33 common and 64 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 64 bit segment latch serially, and then it is stored to 64 bit shift latch. When each common is selected by 33 bit common register, segment data also output through segment driver from 64 bit segment latch.

Cursor/Blink Control Circuit

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

Character code DDRAM data					CGRAM Address						CGRAM Data High byte								CGRAM Data Low byte							
B15~B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	X	0	0	X	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
							0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
							0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
							0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
							0	1	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0
							0	1	1	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
							0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
							1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
							1	0	1	0	0	0	0	1	0	0	1	1	1	1	0	0	1	0	0	0
							1	0	1	1	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0
							1	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0
							1	1	0	1	0	0	0	1	0	0	1	1	1	1	0	0	1	0	0	0
							1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	X	0	1	X	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
							0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
							0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
							0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
							0	1	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0
							0	1	1	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
							0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
							1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
							1	0	1	0	0	0	0	1	0	0	1	1	1	1	0	0	1	0	0	0
							1	0	1	1	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0
							1	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0
							1	1	0	1	0	0	0	1	0	0	1	1	1	1	0	0	1	0	0	0
							1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table1 Relationship between CGRAM addresses, character codes(DDRAM) and character patterns (CGRAM DATA)

NOTES:

1. Character code bits 1 to 2 correspond to CGRAM address bits 4 to 5 (2 bit: 4 types).

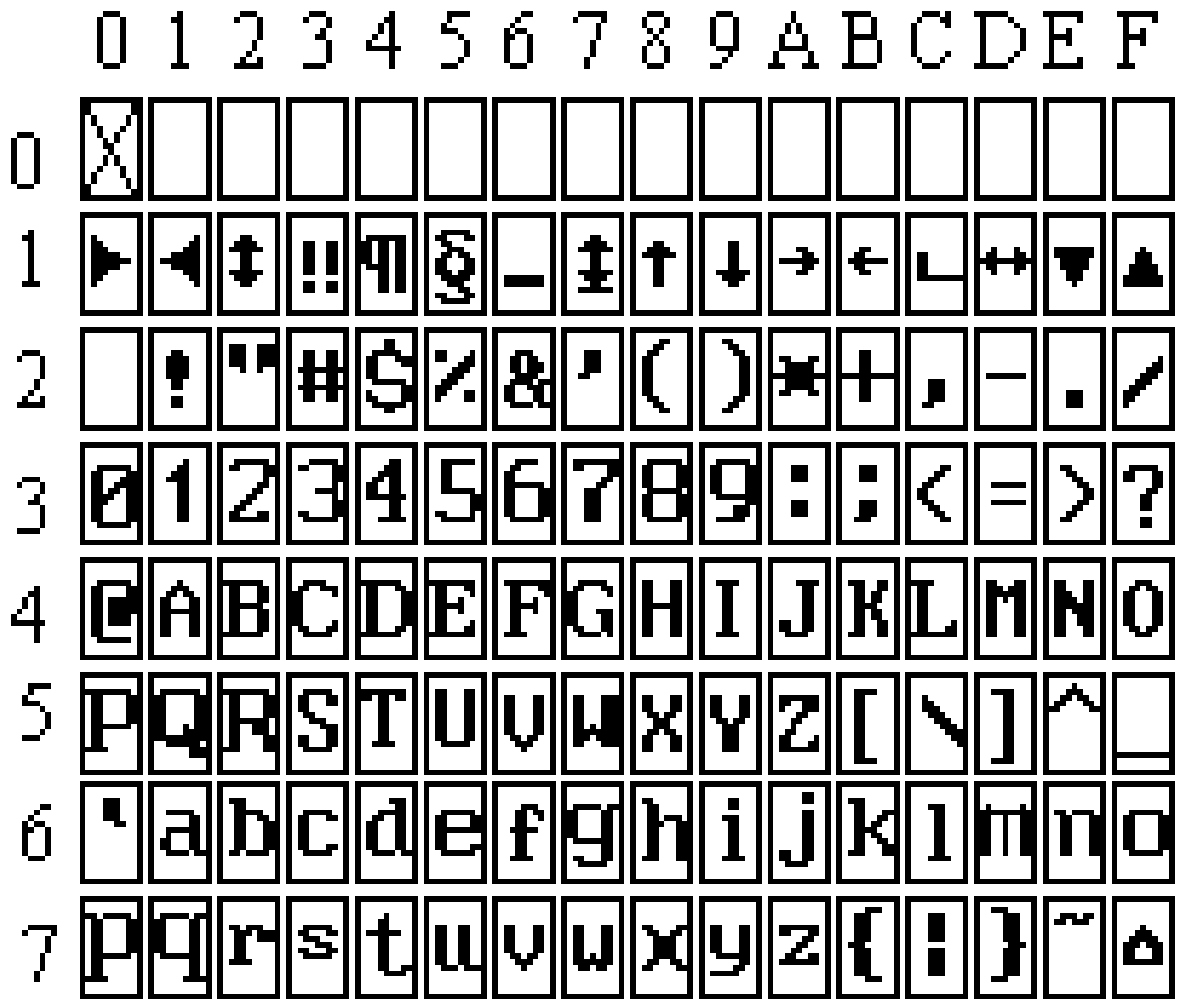
2. CGRAM address bits 0 to 3 designate the character pattern line position. The 16th line is the cursor position and a logical or with the cursor forms its display. Maintain the 16th line data,corresponding to the cursor display position, as to as the cursor display. If the 16th line data is 1,1 bits will light up the 16th line regardless of the cursor presence.

3.Character pattern ROW positions correspond to CGRAM data bits 0 to 15(bit 15 being at the left).

***4.As shown table, CGRAM character patterns are selected when character code bits 4 to 15 are all 0and bit 0 andbit 3are don't care(X).**

Table 6 Relationship between ICON RAM addresses,data and segment pin location bit map.

		ICON RAM Data															
		High Byte								Low Byte							
ICON RAM ADDRESS(AC3——AC0)		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	0	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
	1	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG2	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31
	2	SEG32	SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40	SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47
	3	SEG48	SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56	SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63
	4	SEG64	SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72	SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79
	5	SEG80	SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88	SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95
	6	SEG96	SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104	SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111
	7	SEG112	SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120	SEG121	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
	8	SEG128	SEG129	SEG130	SEG131	SEG132	SEG133	SEG134	SEG135	SEG136	SEG137	SEG138	SEG139	SEG140	SEG141	SEG142	SEG143
	9	SEG144	SEG145	SEG146	SEG147	SEG148	SEG149	SEG150	SEG151	SEG152	SEG153	SEG154	SEG155	SEG156	SEG157	SEG158	SEG159
	A	SEG160	SEG161	SEG162	SEG163	SEG164	SEG165	SEG166	SEG167	SEG168	SEG169	SEG170	SEG171	SEG172	SEG173	SEG174	SEG175
	B	SEG176	SEG177	SEG178	SEG179	SEG180	SEG181	SEG182	SEG183	SEG184	SEG185	SEG186	SEG187	SEG188	SEG189	SEG190	SEG191
	C	SEG192	SEG193	SEG194	SEG195	SEG196	SEG197	SEG198	SEG199	SEG200	SEG201	SEG202	SEG203	SEG204	SEG205	SEG206	SEG207
	D	SEG208	SEG209	SEG210	SEG211	SEG212	SEG213	SEG214	SEG215	SEG216	SEG217	SEG218	SEG219	SEG220	SEG221	SEG222	SEG223
	E	SEG224	SEG225	SEG226	SEG227	SEG228	SEG229	SEG230	SEG231	SEG232	SEG233	SEG234	SEG235	SEG236	SEG237	SEG238	SEG239
	F	SEG240	SEG241	SEG242	SEG243	SEG244	SEG245	SEG246	SEG247	SEG248	SEG249	SEG250	SEG251	SEG252	SEG253	SEG254	SEG255


0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
5
6
7

Display command

The ST7920 which have two categories of instructions that:

- Instruction Tabe: (RE=0:Enable basic instruction.)

Parameter	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Note	Execution time (450khz)
Clear Display	0	0	0	0	0	0	0	0	0	1	write “20H”to DDRAM and set DDRAM address to”00H” from AC	2.5ms
Return home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted.The contents of DDRAM are not change	2.5ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read	60μs
Display on/off	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:Cursor position on	60μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction without changing DDRAM data	60μs
Function Set	0	0	0	0	1	DL	N	0 RE	G	X	DL:interface data is 8/4 bits N=1 & RE=0: 3 Line setting N=1 & RE=1: 4 Line setting G=1: Graphic display on G=0: Graphic display off Others: 2 line setting RE=1: Extended instruction setting RE=0: Normal instruction setting	60μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address cornter	60μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address cornter	60μs
Read Busy Flug and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	wether during internal operation or not can be known by reading BF . the cintents of address counter can also be read.	0μs
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	write data into internal RAM	60μs
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	read data from internal RAM	60μs

l Instruction Table: (RE=1: Enable extension instruction.)

Parameter	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Note	Execution time (450khz)
Standby Mode	0	0	0	0	0	0	0	0	0	1	Enter standby mode, only Icon areas display. Standby mode can be released by any other instructions.	60 us
Start Row Enable	0	0	0	0	0	0	0	0	1	SR	SR=1: Allow change start display Row. SR=0: Disable start display Row change.	60us
Reverse Line Select	0	0	0	0	0	0	0	1	R1	R0	Choice one of 4 lines which data is reverse display.	60 μ s
Sleep mode and Set GRAM page	0	0	0	0	0	0	1	D	C	B	SL=0: Enter sleep mode. SL=1: Wake-up from sleep mode GD: Display graphic page 0 or 1 GW： Write data to graphic page 0 or 1． (Effective while GP=1)	60 μ s
Display Shift by dot	0	0	0	0	0	1	OA	LR	L1	L0	OA=1: One of 4 lines shift enable. OA=0: All line shift enable. LR=1: Dot by dot shift right. LR=0: Dot by dot shift left. L1,L0: Choice one of 4 lines shift	60 μ s
Function Set (Modify)	0	0	0	0	1	CL	N	1 RE	G	GP	CL=1: Select 16 character line CL=0: Select 8 character line N=1 & RE=1: 4 line display RE=1: Extended instruction setting. RE=0: Normal instruction setting. G=1: Graphic display on G=0: Graphic display off GP=1: Two page GRAM GP=0: One page GRAM	60 μ s
Set IRAM or Start Row address	0	0	0	1	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0	SR=1: AC5~AC0 is start row SR=0: AC5~AC0 is ICON RAM address	60 μ s
Set Graphic RAM address	0	0	1	AC 6	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0	Set Graphic RAM address in address counter. Execute once set the address of display row. Execute again set the address of display column. Each address of display column has data of 16 bits. Therefore write data should execute 2 times.	60 μ s

NOTE:

Be sure the ST7920 is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7920. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the

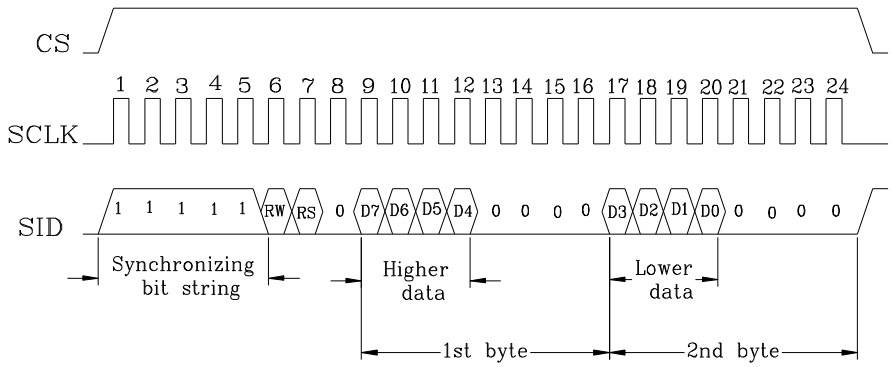
list of each instruction execution time.

8. Serial Interface & Transferring Serial Data

The ST7920 enters serial mode when the PSB pin is set low. A two-line clock synchronous transfer method is used. The ST7920 receives serial input data(SID) by synchronizing with a transfer clock(SCLK) sent from the master side. When the ST7920 interfaces with several chips, chip select pin(CS) must be used. The transfer clock(SCLK) input is activated by making chip select(CS) high. In addition, the transfer counter of the ST7920 can be reset and serial transfer synchronized by making chip select(CS) low. Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In a minimum system where a single ST7920 interfaces to a single MPU, an interface can be constructed from the transfer clock(SCLK) and serial input data(SID). In this case, chip select(CS) should be fixedto high.

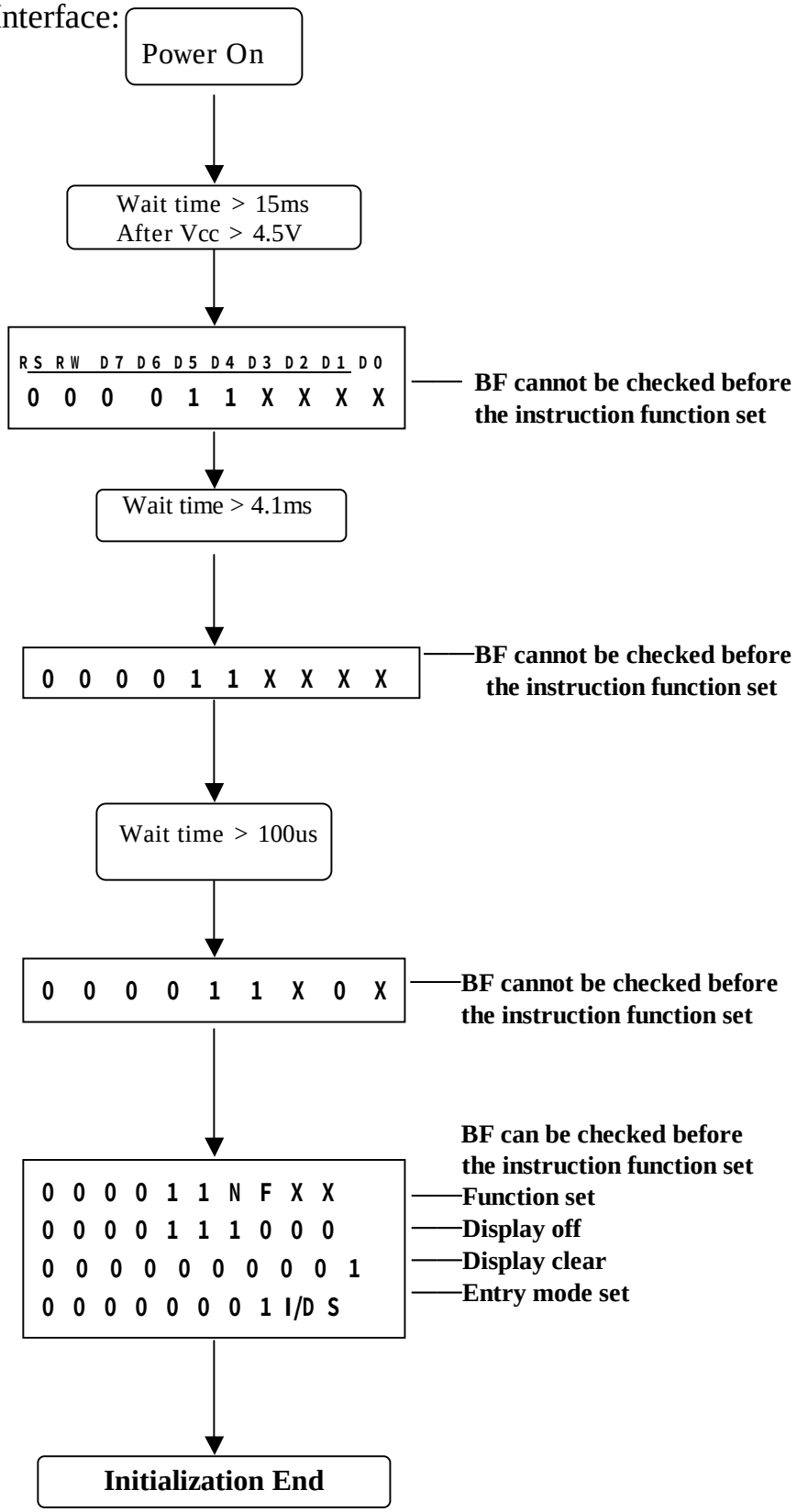
The transfer clock(SCLK) is independent of operational clock of the ST7920. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock must be considered since the ST7920 does not have an internal transmit/receive buffer. Following figure shows the basic procedure for transferring serial data. To begin with, transfer the start byte. By receiving five consecutive bits of 1(synchronizing bit string) at the beginning of the start byte, the transfer counter of the ST7920 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string(5 bits) specify transfer direction(RW bit) and register select(RS bit). Be sure to transfer 0 in the 8 th bit.

After receiving the start synchronizing bit string, the RW bit(=0), and RS bit in the start byte, an 8-bit instruction is received in 2 bytes: the higher 4 bits of the instruction are placed in the LSB of the first byte, and the lower 4 bits of the instruction are placed in the LSB of the second byte. Be sure to transfer 0 in the following 4 bits of each byte.

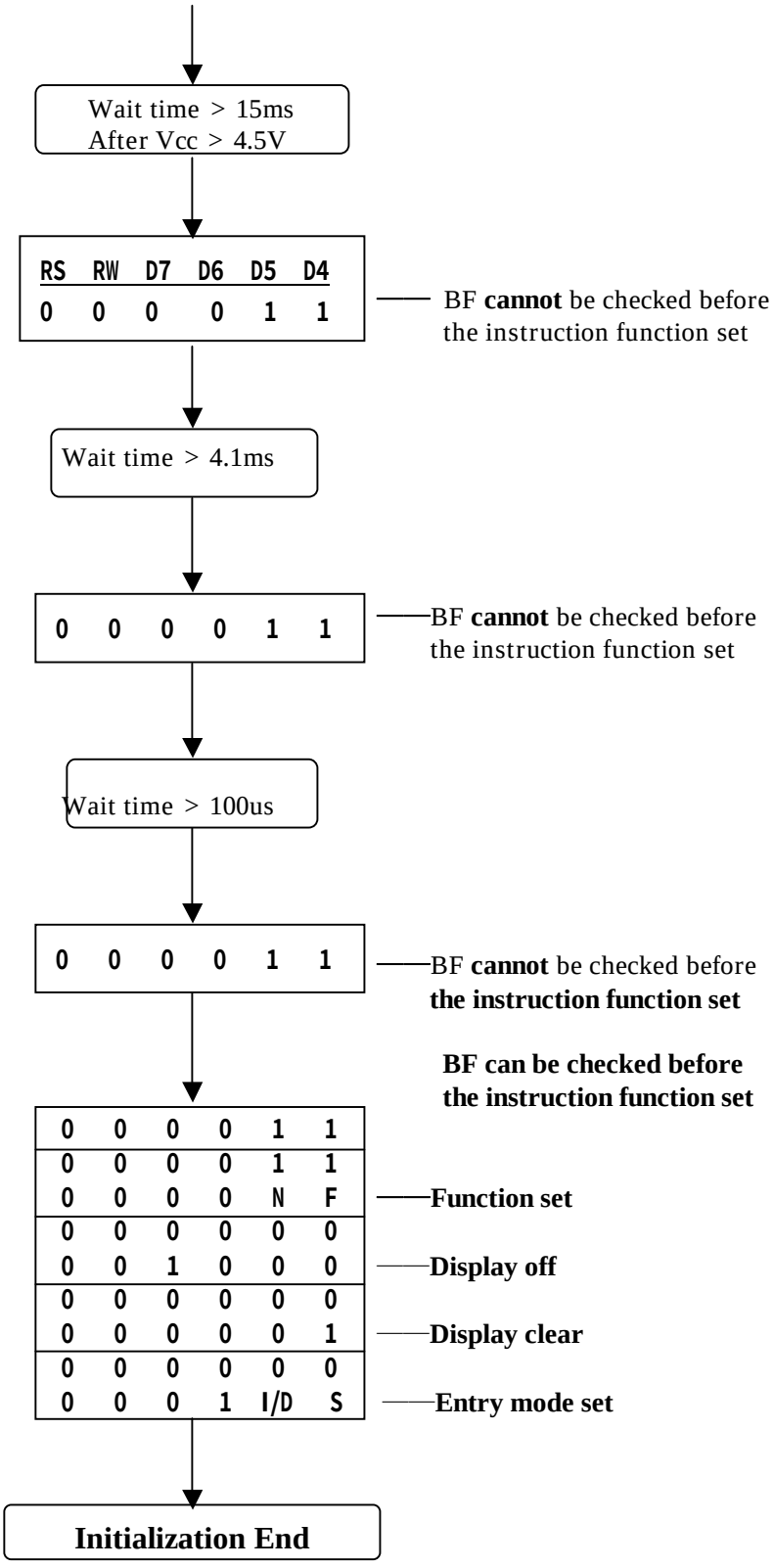


9. Initializing by instruction

- 8-bit Interface:



- **4-bit Interface** **Power On**


Wait time > 15ms
After Vcc > 4.5V
RS RW D7 D6 D5 D4
0 0 0 0 1 1
BF cannot be checked before the instruction function set
Wait time > 4.1ms
0 0 0 0 1 1
BF cannot be checked before the instruction function set
Wait time > 100us
0 0 0 0 1 1
BF cannot be checked before the instruction function set
BF can be checked before the instruction function set
0 0 0 0 1 1
0 0 0 0 1 1
0 0 0 0 N F
Function set
0 0 0 0 0 0
0 0 1 0 0 0
Display off
0 0 0 0 0 0
0 0 0 0 0 1
Display clear
0 0 0 0 0 0
0 0 0 1 I/D S
Entry mode set
Initialization End

7. ST7920 BIG-5 中文字型码表